



ACTT4S-800E

AC Thyristor Triac power switch

Rev. 1 — 29 March 2012

Product data sheet

1. Product profile

1.1 General description

Planar passivated AC Thyristor Triac power switch in a SOT428 (DPAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

1.2 Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Sensitive gate for easy logic level triggering
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

1.3 Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$; $t_{\text{p}} = 20\text{ ms}$; see Figure 5 ; see Figure 6	-	-	35	A
T_{j}	junction temperature		-	-	125	°C
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{mb}} \leq 108\text{ °C}$; see Figure 1 ; see Figure 2 ; see Figure 4	-	-	4	A

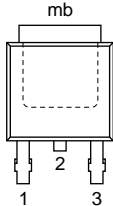
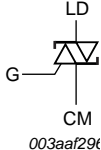


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PP}	peak pulse voltage	T _j = 25 °C; non-repetitive, off-state; see Figure 3	-	-	2	kV
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; see Figure 8	-	-	10	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; see Figure 8	-	-	10	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; see Figure 8	-	-	10	mA
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C	850	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; see Figure 13	500	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 1 V/μs; gate open circuit; see Figure 14 ; see Figure 15	8	-	-	A/ms

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common		
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

SOT428 (DPAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
ACTT4S-800E	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 108\text{ °C}$; see Figure 1 ; see Figure 2 ; see Figure 4	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; see Figure 5 ; see Figure 6	-	35	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	39	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	6	A ² s
di_T/dt	rate of rise of on-state current	$I_T = 6\text{ A}$; $I_G = 0.2\text{ A}$; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	100	A/ μs
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25\text{ °C}$; non-repetitive, off-state; see Figure 3	-	2	kV

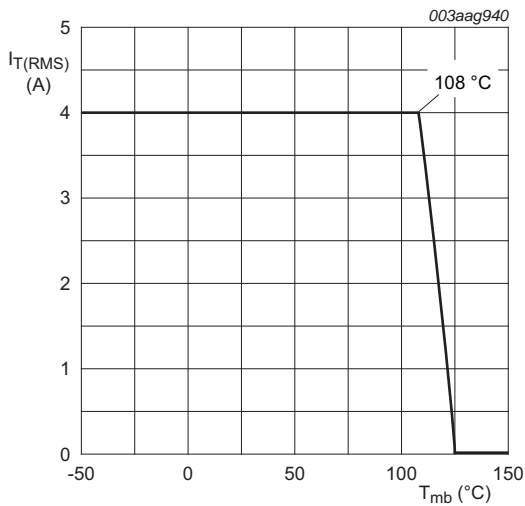
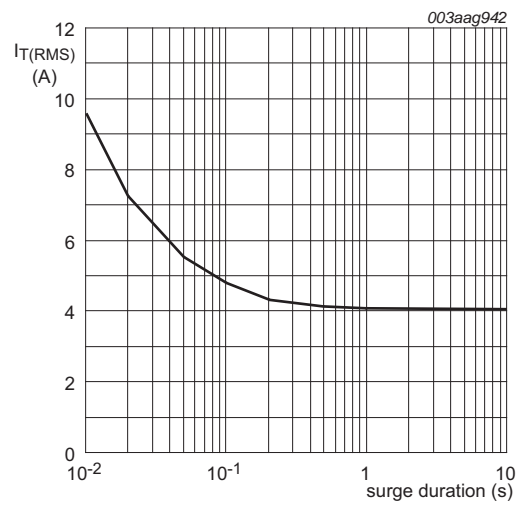


Fig 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50\text{ Hz}$; $T_{mb} = 108\text{ °C}$

Fig 2. RMS on-state current as a function of surge duration; maximum values

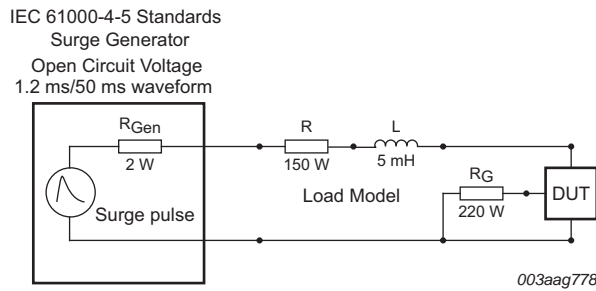


Fig 3. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

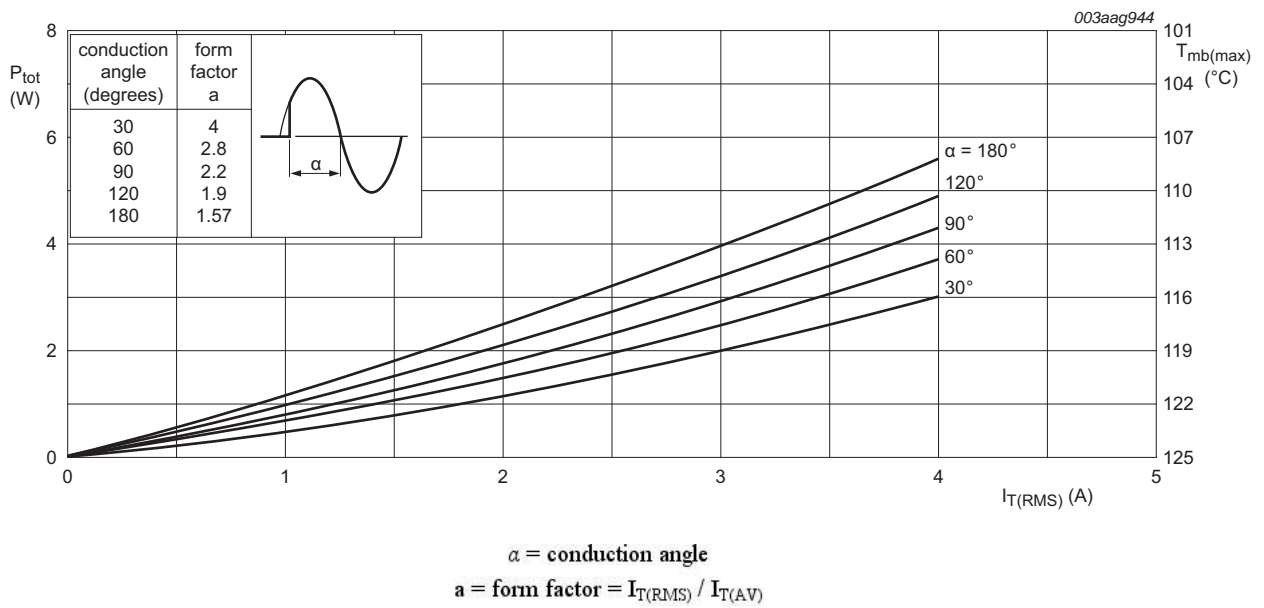


Fig 4. power dissipation as a function of RMS on-state current; maximum values

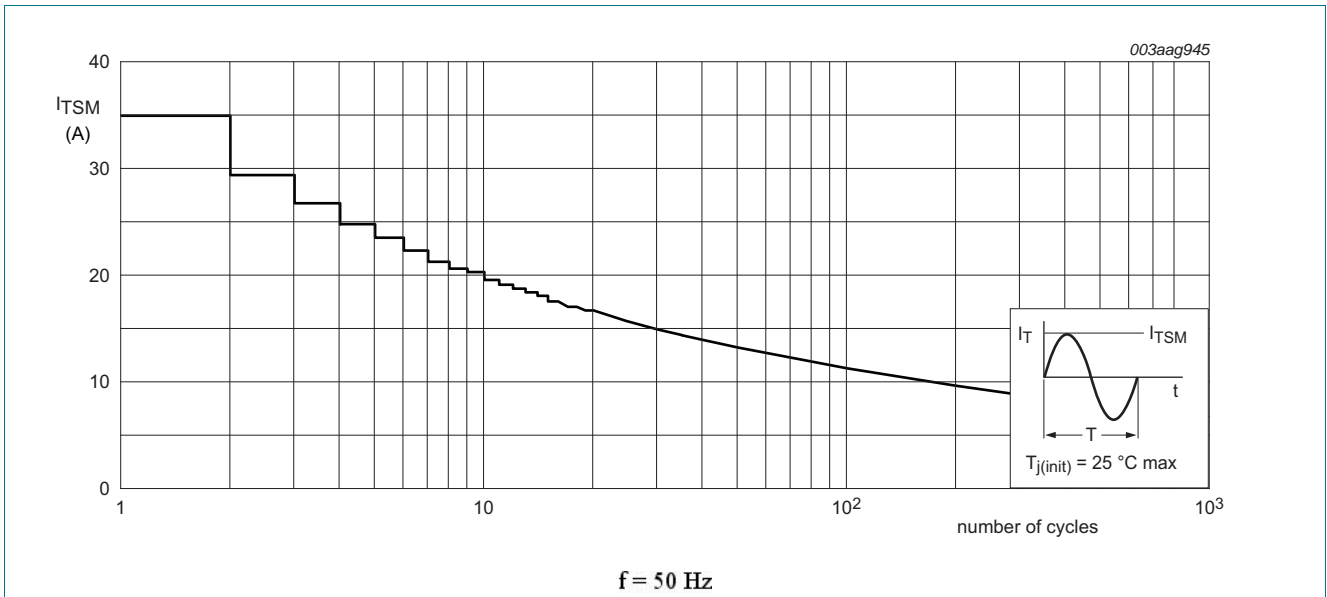


Fig 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

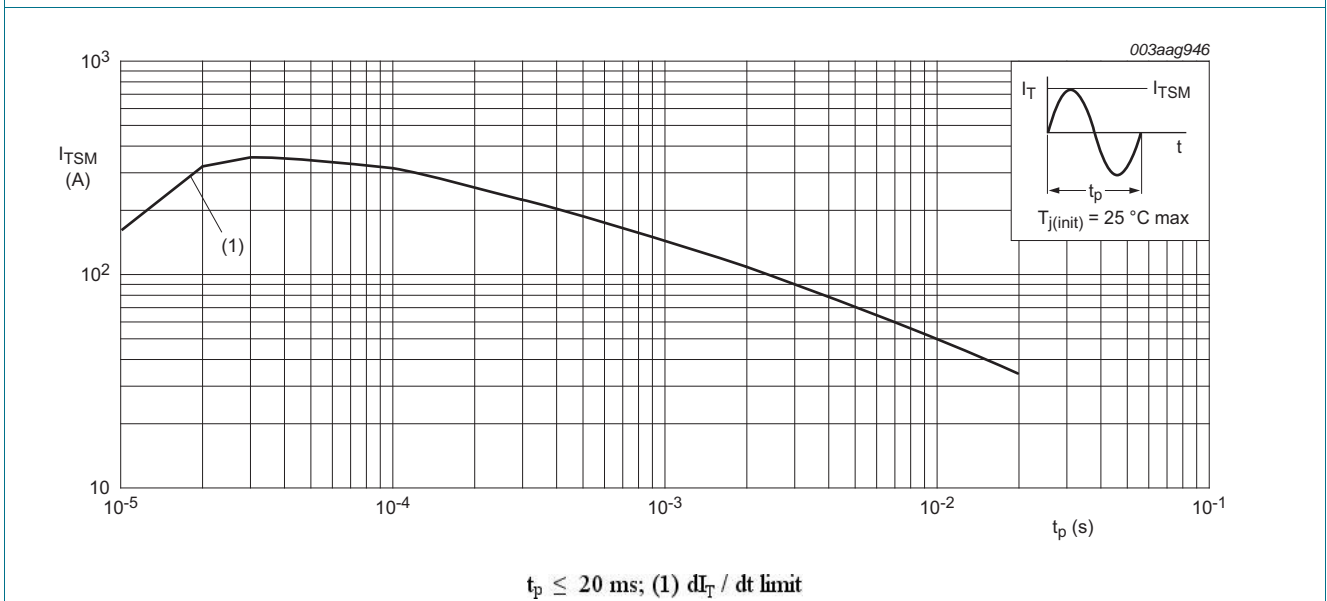
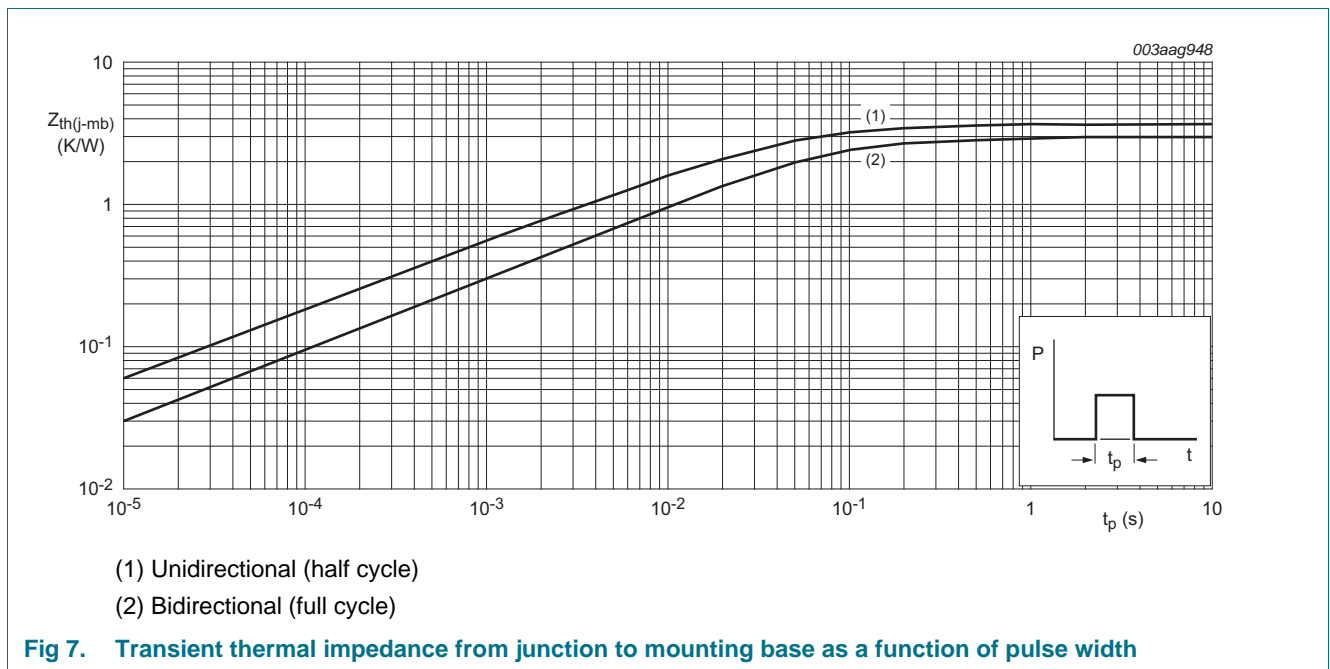


Fig 6. Non-repetitive peak on-state current as a function of pulse width; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

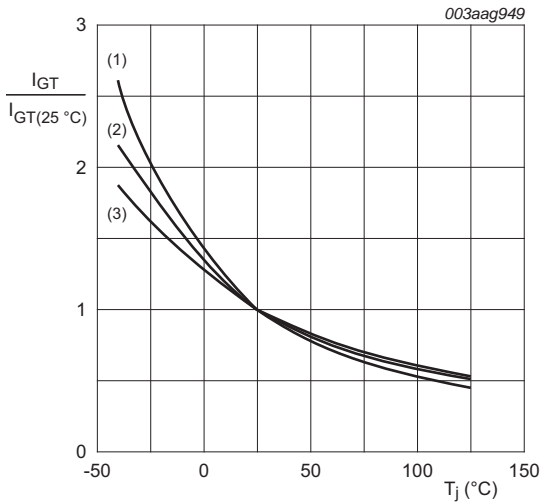
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; see Figure 7	-	-	3	K/W
		half cycle; see Figure 7	-	-	3.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	75	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; see Figure 8	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; see Figure 8	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; see Figure 8	-	-	10	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; see Figure 9	-	-	30	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; see Figure 9	-	-	40	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; see Figure 9	-	-	30	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; see Figure 10	-	-	20	mA
V_T	on-state voltage	$I_T = 6\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11	-	-	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$; see Figure 12	-	-	1.5	V
		$V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 125\text{ °C}$; see Figure 12	0.2	-	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ °C}$	-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	-	0.5	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ °C}$	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; see Figure 13	500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 4\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit; see Figure 14 ; see Figure 15	4	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 4\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit; see Figure 14 ; see Figure 15	5	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 4\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit; see Figure 14 ; see Figure 15	8	-	-	A/ms



- (1) LD- G-
- (2) LD+ G+
- (3) LD+ G-

Fig 8. Normalized gate trigger current as a function of junction temperature

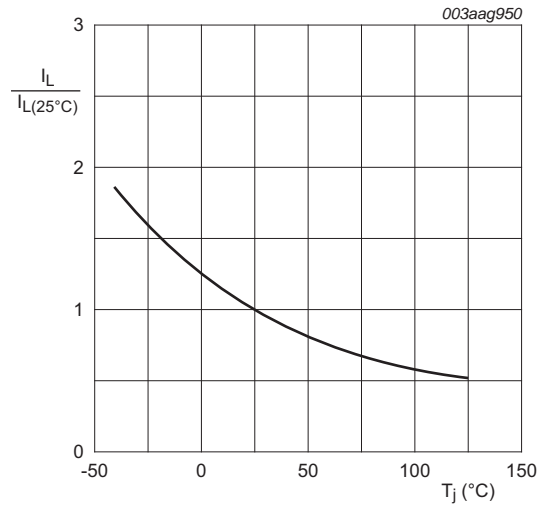


Fig 9. Normalized latching current as a function of junction temperature

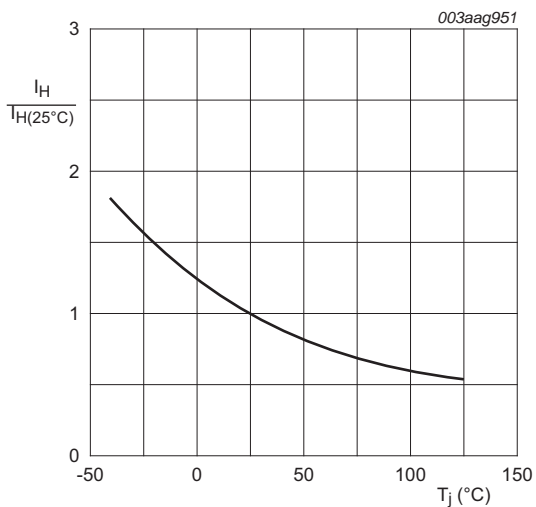
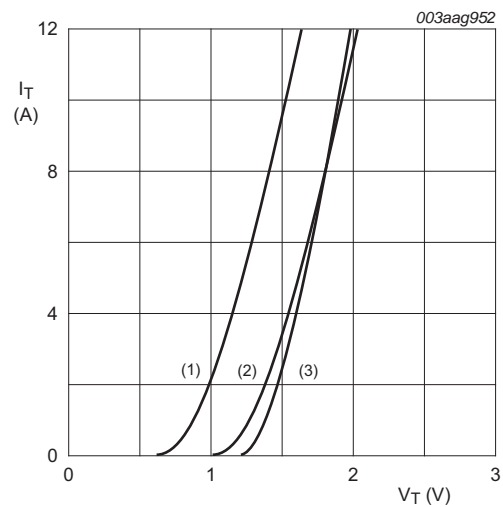


Fig 10. Normalized holding current as a function of junction temperature



$V_o = 1.242 \text{ V}; R_s = 0.074 \Omega$

- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
- (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
- (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig 11. On-state current as a function of on-state voltage

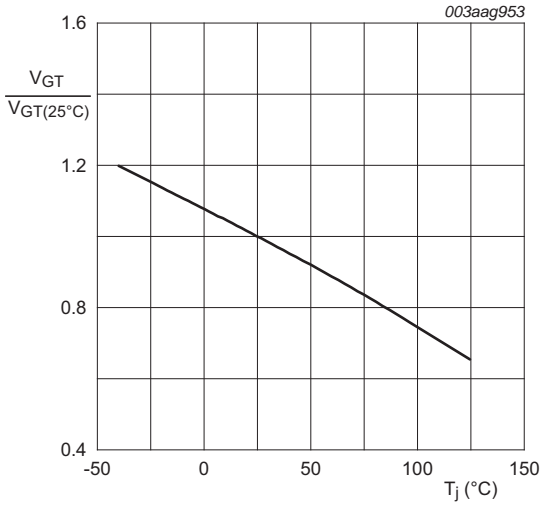
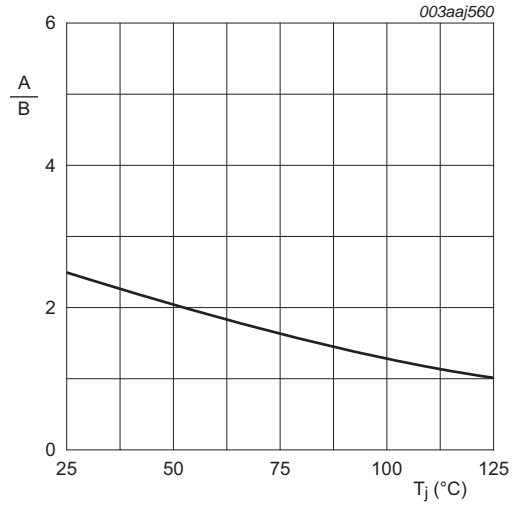
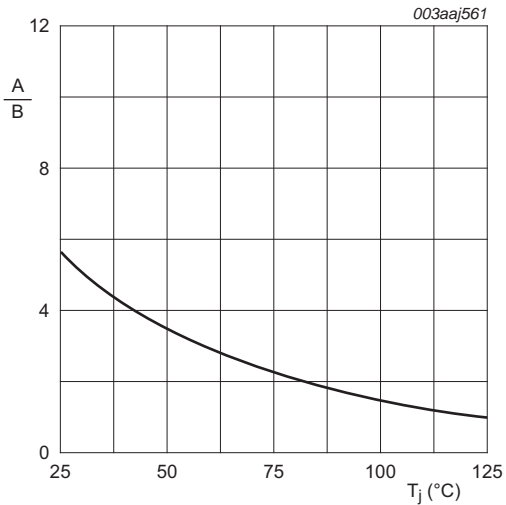


Fig 12. Normalized gate trigger voltage as a function of junction temperature



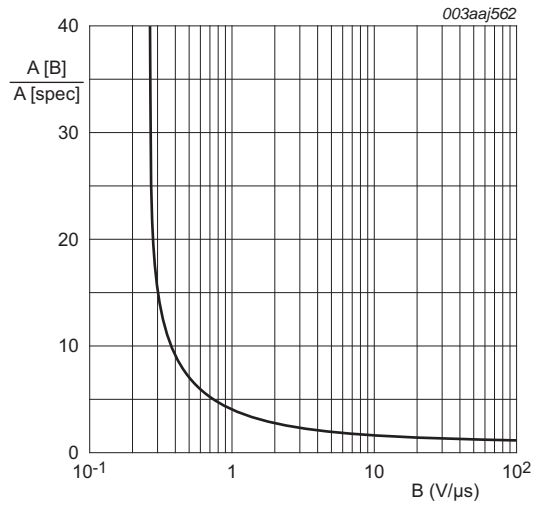
A is dV_D/dt at condition T_j $^{\circ}\text{C}$
 B is dV_D/dt at condition T_j 125 $^{\circ}\text{C}$

Fig 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A is di_{com}/dt at condition T_j $^{\circ}\text{C}$
 B is di_{com}/dt at condition T_j 125 $^{\circ}\text{C}$
 $V_D = 400$ V

Fig 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A[B] is di_{com}/dt at condition B, dV_{com}/dt
 A[spec] is the specified data sheet value of di_{com}/dt
 turn-off time < 20 ms

Fig 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

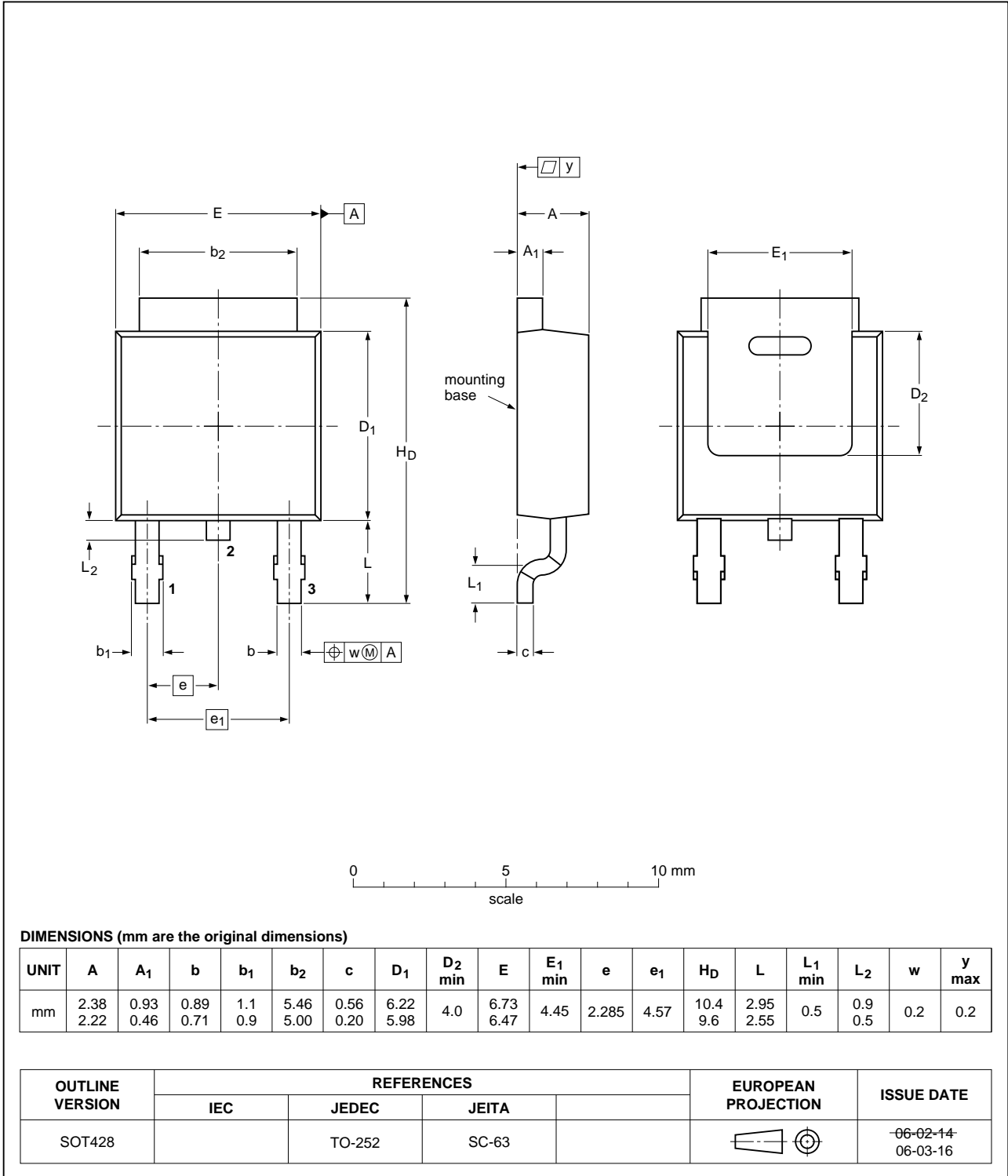


Fig 16. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ACTT4S-800E v.1	20120329	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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